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23 ALPHA & OMEGA SEMICONDUCTOR,
24 INC.

25 UNITED STATES DISTRICT COURT
26 NORTHERN DISTRICT OF CALIFORNIA
27 SAN FRANCISCO DIVISION

28 ALPHA & OMEGA SEMICONDUCTOR,
LTD., a Bermuda corporation; and
ALPHA & OMEGA SEMICONDUCTOR,
INC., a California corporation,

Plaintiffs and Counterdefendants,

v.

FAIRCHILD SEMICONDUCTOR
CORP., a Delaware corporation,

Defendant and Counterclaimant.

AND RELATED COUNTERCLAIMS.

Case No. C 07-2638 JSW
(Consolidated with Case No. C-07-2664 JSW)

**DECLARATION OF C. ANDRE T.
SALAMA, PH.D. IN SUPPORT OF ALPHA
& OMEGA SEMICONDUCTOR, LTD AND
ALPHA & OMEGA SEMICONDUCTOR,
INC'S OPPOSITION CLAIM
CONSTRUCTION BRIEF**

Date: June 4, 2008
Time: 2:00 PM
Place: Courtroom 2, 17th Floor
Judge: Honorable Jeffrey S. White

1 I, C. Andre T. Salama, hereby declare as follows:

2 1. I am a University Professor (Emeritus) at the University of Toronto in the
3 Department of Electrical and Computer Engineering, 10 King's College Road, Toronto, Ontario,
4 M5S 3G4, Canada. I have been retained as a consultant for the Plaintiffs and counterdefendants
5 Alpha & Omega Semiconductor, LTD and Alpha & Omega Semiconductor, Inc., in the present
6 action. I submit this declaration in support of Alpha & Omega Semiconductor, LTD and Alpha &
7 Omega Semiconductor, Inc.'s Opposition Claim Construction Brief Pursuant to Civil L. R. 16-
8 11(d)(1).

9 2. A semiconductor p-n junction is the area of transition between two semiconductor
10 regions of opposite conductivity type (p and n).

11 3. The region near the p-n junction, the transition region, is known as the "depletion
12 region" since the mobile carriers (electrons and holes) in that region are effectively reduced in
13 number or depleted as compared to the bulk regions away from the junction. At equilibrium the
14 fixed charges in the depletion region on either side of the junction cancel each other out. Under
15 reverse bias conditions, the width of the depletion regions increases leading to an increase of the
16 electric field across the junction. Once the field across the junction exceeds a critical value,
17 avalanche breakdown occurs at the junction.

18 4. "Avalanche breakdown" is an unwanted process which occurs in a power
19 MOSFET when a sufficiently high voltage (the breakdown voltage) is applied to the drain of the
20 device causing the electric field across the reverse biased depletion region of the p body/n-
21 epitaxial junction to exceed a critical value. Due to the high electric field, the velocity of carriers
22 crossing the depletion layer increases and when they collide with the semiconductor lattice they
23 free additional carriers resulting in a regenerative or avalanching process which causes the current
24 across the device to increase independent of the voltage applied to the drain (even when the
25 device is turned off). Avalanche breakdown can damage the gate oxide layer covering the
26 interior surface of the gate trenches.

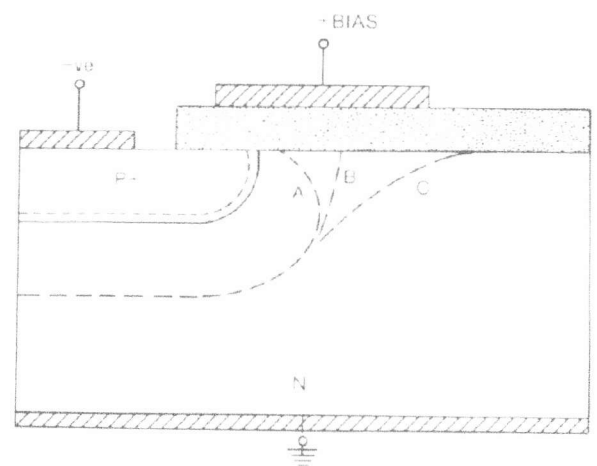
27 5. The breakdown initiation occurs at the p-n junction where the electric field is
28 highest. Designers skilled in the field of semiconductor devices are concerned with controlling

1 the location of breakdown initiation and with the avalanche current at breakdown initiation. The
 2 breakdown recited in the claims of the Mo patents refers to breakdown at initiation, otherwise the
 3 claims could encompass any doping profile, since breakdown at the p body/n-epitaxial interface
 4 could occur practically anywhere in the device.

5 6. If increasing voltage is applied to a MOSFET after breakdown initiation,
 6 breakdown can spread rapidly among the cells; within each cell, breakdown can start at one point
 7 in the cell, and then, as the voltage is increased, spread to other parts of the cell. If enough
 8 voltage is applied after breakdown initiation, current-paths can form through any number of
 9 undesired pathways within the transistor.

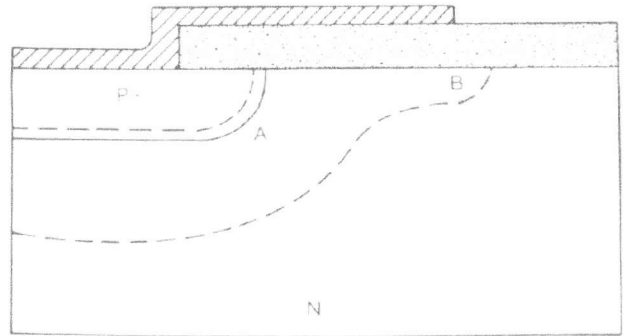
10 7. The “termination region” of a power MOSFET is the portion of the die that
 11 generally includes termination structures (for example, field plate, channel stop and field ring)
 12 surrounding the active region of the device. These termination structures help to increase the
 13 power MOSFET’s breakdown voltage by modifying the depletion layer between the p-well (body
 14 region) and the n epitaxial region (drain) of the device.

15 8. In the active region of a power MOSFET, the depletion layer between, for
 16 example, the p-type well and the n-type epilayer runs parallel to the substrate surface. If there
 17 were no edge termination structure, the edge of the depletion layer would curve around the end of
 18 the p-type well in the termination region, as
 19 shown by the dotted line B in Figure 3.44 shown
 20 on page 117 of Modern Power Devices by B.
 21 Jayant Baliga (the “Baliga text”), which is
 22 reproduced to the right. The curvature of the
 23 depletion layer at the surface of the termination
 24 region affects the MOSFET breakdown voltage.
 25 Generally, the higher the depletion layer curvature
 26 the lower breakdown voltage and *vice versa*.



27 9. A field plate is a termination structure in a power MOSFET that modifies the
 28 depletion layer in the underlying silicon termination region of the device and thereby reduces the

depletion layer's curvature. The dotted line B in Baliga's Fig. 3.45, shown on the right, illustrates how a negative voltage applied to the field plate reduces the curvature of the depletion layer thereby increasing the breakdown voltage of the device.



10. In the field of semiconductor devices the terms “abrupt” and “linearly” graded junctions are well defined (see Physics of Semiconductor Devices by S.M. Sze: the “Sze text”). A linearly graded junction is a p-n junction in which the change from p-type dopants to n-type dopants is gradual. The structural difference between linearly graded and abrupt junctions is the concentration gradient between the two regions: an abrupt junction has a concentration gradient that is very steep (essentially 90 degrees), and a linearly graded junction has a more angled concentration gradient (less than 90 degrees).

11. As suggested by Fairchild's Dr. Blanchard, the difference between an abrupt junction and a linearly graded junction may be visualized by the analogy of a curb between a sidewalk and a street. As defined by the Mo patents' inventors, and consistent with the Sze text, a junction is abrupt when the curb falls steeply from the sidewalk to the street, and is linearly graded when it descends as a ramp. Dr. Blanchard, however, suggests that both the steep curb and the ramp qualify as abrupt junctions because both have multiple gradients at the edges formed at the top and bottom where they intersect the sidewalk and street. This is inconsistent with the prosecution history and Dr. Blanchard's own original analogy.

12. Fairchild's proposed definition of “abrupt junction” including the phrase “short relative to the depth of the well” does not clearly define the term and provides no objective measure of what constitutes an abrupt junction. Furthermore, it is not clear from the patent why the depth of the well is relevant to whether or not a junction between the well and another region is abrupt. To use Dr. Blanchard's curb analogy, one would not consider a ramp to be abrupt

1 merely because it borders on a large street, nor would one consider a steep curb to be linearly
2 graded merely because it borders on a narrow alley.

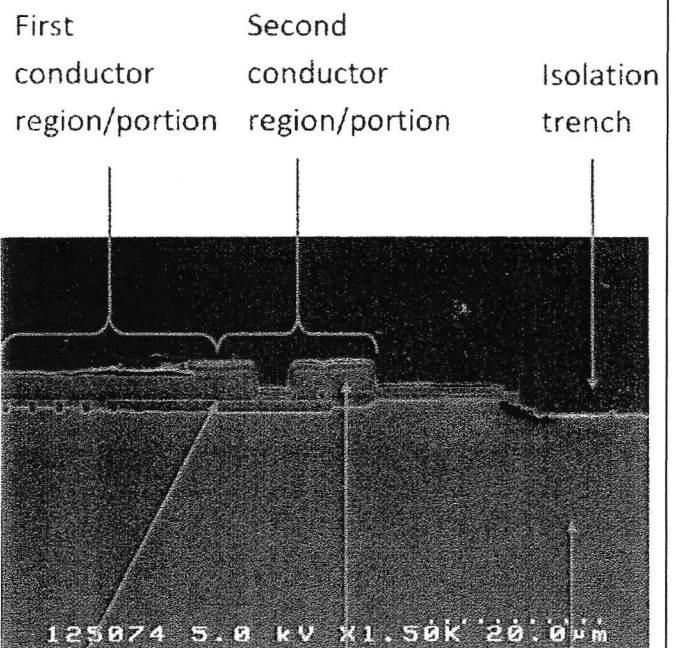
3 13. The definition of “abrupt junction” proposed by AOS is how one familiar with the
4 field of semiconductor devices would interpret the term, especially in light of the specification
5 and prosecution history of the Mo patents. In addition, this definition can be applied objectively
6 using computer simulations or repeated experiments commonly performed in the semiconductor
7 field.

8 14. A transition from a highly doped region to a lower doped region of the same
9 conductivity type (e.g., p^+ -p) is called a high-low junction. A high-low junction is much different
10 from the widely studied p-n junction. One significant difference between p-n junctions and high-
11 low junctions is that avalanche breakdown only occurs at p-n junctions. A high-low junction, in
12 contrast, functions as an ohmic contact that allows current to flow freely in either direction.
13 Because of the free flow of current, there is no avalanche breakdown at a high-low junction.
14 Therefore, when avalanche breakdown occurs in an active cell of a power MOSFET, as described
15 in the Mo patents, the breakdown occurs at the p-n junction between the p body and the n-
16 epitaxial layer. There is no avalanche breakdown at the high-low junction between the heavy
17 body and the well located above the p-n junction.

18 15. Although AOS’s definition of “abrupt junction” is how one in the field of
19 semiconductor devices would interpret the term, one cannot determine whether a given design has
20 an abrupt junction as that term is defined and used by the inventors of the Mo patents. The
21 specification of the Mo patents teaches that an abrupt junction refers to a high-low junction
22 between the p^+ heavy body and the p-well, that is, a transition between two regions of the same
23 conductivity type. However, during prosecution of the Mo patents the inventors defined the term
24 “abrupt junction,” on pages 5 – 7 of their June 7, 2001 response to the Patent & Trademark Office
25 (“PTO”), with repeated references to section 2.3.1 of the Sze text. The Sze text and the definition
26 given to the term abrupt junction by the applicants during prosecution of the Mo patents refers to
27 a p-n junction, that is, a transition between regions of opposite conductivity types. Because the

1 inventors' definition of "abrupt junction" during prosecution is inconsistent with the teaching of
2 the specification, one cannot determine whether a given design has an abrupt junction.

3 16. An "isolation trench" is sometimes included as part of the termination region of
4 the power MOSFET to prevent unwanted leakage of current in the periphery of the device or in
5 adjoining devices. By physically separating the upper surface of the body region from the die
6 edge of the MOSFET with a trench filled with an insulating, or "dielectric," material, the isolation
7 trench prevents leakage current from the body region to the drain at the die edge. Fairchild's
8 suggested definition of an isolation trench
9 as an "insulating structure" is vague, and
10 could encompass insulating structures that
11 are not trenched. In addition, the structure
12 labeled "Isolation trench" in Fig. AO6405-6
13 of Fairchild's Preliminary Infringement
14 Contentions, shown to the right, does not
15 appear, from this image, to be an isolation
16 trench. First, the image does not show two
17 sidewalls. Second, the image does not
18 show visible insulating material filling the
19 structure.



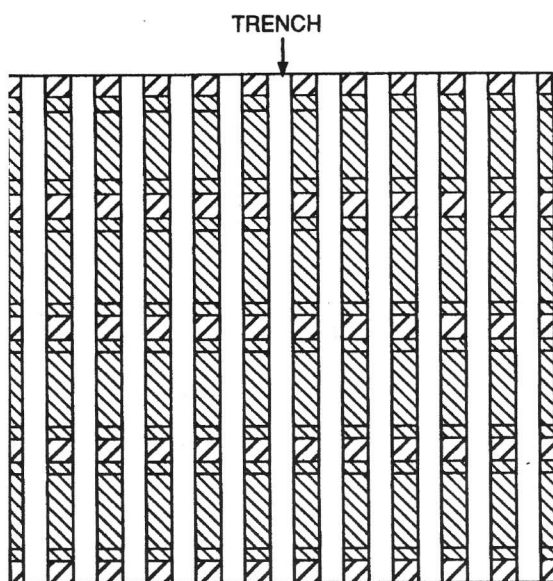
20 17. A "trench" is commonly understood, by those skilled in the art of semiconductor
21 device fabrication, according to its common, non-technical meaning. That is, a trench is a
22 structure that extends into the substrate and is defined by two sidewalls and a bottom. Fairchild's
23 proposed construction of a trench as a structure with one wall would be a wall or a step, not a
24 trench.

25 18. Individual power transistor dies must be separated from the wafer after fabrication.
26 Commonly, the wafer is placed in a holder on a sticky Mylar sheet and automatically scribed in
27 both the x and y directions using a high speed diamond saw. Scribing borders typically in the
28 range of 75 μ m to 250 μ m are formed around the periphery of the die during fabrication. These

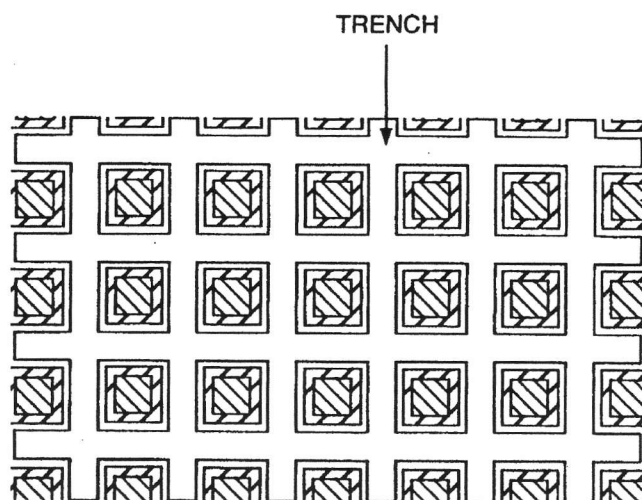
1 borders are left free of oxide to facilitate the scribing process. These “scribe lines” are shallow
2 grooves cut in the silicon surface of the wafer and used to facilitate the separation of the
3 individual dies. Following scribing, the wafer is removed from the holder and rollers are used to
4 apply pressure to the wafer causing it to fracture along the scribe lines to separate the dies.
5 Alternatively, the diamond saw can be used to cut completely through the wafer and separate the
6 dies.

7 19. Semiconductor device manufacturers do not normally cut through isolation
8 trenches filled with oxide because of the difficulty of scribing or cutting through the oxide in the
9 trenches and because the trenches would need to be very wide and of the order of 75 to 250 μ m
10 (as compared to typical isolation trenches which are 1-3 μ m wide) to accommodate the width of
11 the diamond saw. Furthermore, cutting through the trenches using a diamond saw increases the
12 likelihood of mechanical damage to the isolation trench.

13 20. An open-cell MOSFET includes multiple, elongated trenched gates arranged in a
14 “stripe” pattern. These elongated trenched gates, also called “inner runners,” extend in one and
15 only one direction because they are parallel to each other. A closed-cell MOSFET includes
16 multiple trenched gates arranged in a grid-like pattern. The figures below illustrate these two
17 different configurations:
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Open-Cell Design



Closed-Cell Design

I declare under of penalty of perjury that the foregoing is true and correct.

Dated: March 27, 2008

by *C. Andre T. Salama*
C. Andre T. Salama, Ph.D.